Amendments to the Claims

1. (Currently Amended) An apparatus ~~for generating clock pulses using a Direct Digital Synthesizer (DDS), the apparatus~~ comprising:

a ~~DDS~~ Direct Digital Synthesizer (DDS) comprising:

a Phase Locked Loop (PLL) multiplier ~~for receiving~~ configured to convert a system reference clock ~~pulses~~ signal of a ~~first~~ system reference clock frequency ~~and converting the system reference clock pulses~~ into a DDS operation clock ~~signals~~ signal of a ~~second~~ DDS operation clock frequency;

a phase accumulator ~~for receiving a Frequency Tuning Word (FTW)~~ configured to operate using the DDS operation clock signal, ~~accumulating~~ accumulate a phase ~~by the FTW~~ using a Frequency Tuning Word (FTW), and ~~outputting the~~ output an accumulated phase of a ~~desired~~ particular frequency~~, wherein the phase accumulator operates using the DDS operation clock signals from the PLL multiplier~~;

a phase-to-magnitude converter ~~for, in responsive to the accumulated phase of the particular frequency from the phase accumulator, providing~~ configured to operate using the DDS operation clock signal and generate a ~~clock~~ sinusoidal signal of the particular frequency having a magnitude corresponding to the accumulated phase of the particular frequency~~, wherein the phase-to-magnitude operates using the DDS operation clock signals from the PLL multiplier~~; and

a Digital-to-Analog (DA) converter ~~for, in responsive to the clock signal from the phase-magnitude converter, converting~~ configured to operate using the DDS operation clock signal from the PLL multiplier and convert the ~~clock~~ sinusoidal signal of the particular frequency to an analog signal of a DDS output frequency, ~~wherein the DA converter operates using the DDS operation clock signals from the PLL multiplier~~;

a band pass filter ~~for bandpass-filtering~~ configured to pass the analog signal of the DDS output frequency from the DA converter ~~to provide a bandpass-filtered signal~~ over a particular frequency band of the DDS output frequency; and

a comparator ~~for, in responsive to the bandpass-filtered signal from the band pass filter, transforming~~ configured to transform the passed analog signal ~~of the DDS output frequency~~ into a square wave signal and output the square wave signal.

2. (Currently Amended) The apparatus of claim 1, wherein the ~~Phase Locked Loop (PLL)~~ PLL multiplier is a 10x PLL multiplier~~, and wherein the first frequency of the system reference clock pulses is 19.6608 MHz and the second frequency of the DDS operation clock signals is 196.608 MHz~~.

3. (Currently Amended) The apparatus of claim 1, wherein the FTW is derived from equations (1) and (2) below,

$$f_{out} = (W*f_{clk})/2^N \quad (1)$$

$$W = \mathrm{INT}[(f_{out}/f_{clk})*2^N] \quad (2)$$

where f_{out} is [[a]] the DDS output frequency, W is a binary value for the FTW, f_{clk} is [[a]] the DDS operation clock frequency, N is the number of input bits of the phase accumulator, and INT[] denotes an integer part of the bracketed expression.

4. (Currently Amended) The apparatus of claim 1, wherein the square wave signal has a low jitter.

5. (New) The apparatus of claim 1, wherein the system reference clock frequency is 19.6608 MHz and the DDS operation clock frequency is 196.608 MHz.

6. (New) The apparatus of claim 1, wherein the bandpass filter is further configured to remove spurious signals and harmonics signals from the analog signal.

7. (New) The apparatus of claim 1, wherein the comparator has a zero-crossing threshold.

8. (New) The apparatus of claim 3, wherein the binary value for the FTW comprises 010011001100110011001100110011001100110011001101, the number of input bits of the phase accumulator comprises 48, and the output frequency comprises 58.9824 MHz.

9. (New) An apparatus comprising:

means for frequency multiplying a system reference clock signal of a system reference clock frequency to generate an operation clock signal of an operation clock frequency;

means for accumulating a phase using a Frequency Tuning Word (FTW) to provide an accumulated phase of a particular frequency, wherein the means for accumulating operates using the operation clock signal;

means for generating a sinusoidal signal of the particular frequency having a magnitude corresponding to the accumulated phase of the particular frequency, wherein the means for generating operates using the operation clock signal;

means for converting the sinusoidal signal of the particular frequency to an analog signal of an output frequency, wherein the means for converting operates using the operation clock signal;

means for passing the analog signal of the output frequency over a particular frequency band of the output frequency; and

means for transforming the passed analog signal into a square wave signal.

10. (New) The apparatus of claim 9, wherein frequency multiplying the system reference clock signal to generate the operation clock signal comprises multiplying the system reference clock frequency by a factor of 10.

11. (New) The apparatus of claim 9, wherein the FTW is derived from equations (1) and (2) below,

$$f_{out} = (W*f_{clk})/2^N \quad (1)$$

$$W = \mathrm{INT}[(f_{out}/f_{clk})*2^N] \quad (2)$$

where f_{out} is the output frequency, W is a binary value for the FTW, f_{clk} is the operation clock frequency, N is the number of input bits of the phase accumulator, and INT[] denotes an integer part of the bracketed expression.

12. (New) The apparatus of claim 11, wherein the binary value for the FTW comprises 010011001100110011001100110011001100110011001101, the number of input bits of the phase accumulator comprises 48, and the output frequency comprises 58.9824 MHz.

13. (New) The apparatus of claim 9, wherein the square wave signal has a low jitter.

14. (New) The apparatus of claim 9, wherein the system reference clock frequency is 19.6608 MHz and the operation clock frequency is 196.608 MHz.

15. (New) A method comprising:

frequency multiplying a system reference clock signal of a system reference clock frequency to provide an operation clock signal of an operation clock frequency;

using the operation clock signal, accumulating a phase using a Frequency Tuning Word (FTW) to provide an accumulated phase of a particular frequency;

using the operation clock signal, generating a sinusoidal signal of the particular frequency having a magnitude corresponding to the accumulated phase of the particular frequency;

using the operation clock signal, converting the sinusoidal signal of the particular frequency to an analog signal of an output frequency;

passing the analog signal of the output frequency over a particular frequency band of the output frequency; and

transforming the passed analog signal into a square wave signal.

16. (New) The method of claim 15, wherein frequency multiplying the system reference clock signal to generate the operation clock signal comprises multiplying the system reference clock frequency by a factor of 10.

17. (New) The method of claim 15, wherein the FTW is derived from equations (1) and (2) below,

$$f_{out} = (W * f_{clk})/2^{N} \quad (1)$$

$$W = \mathrm{INT}[(f_{out}/f_{clk}) * 2^{N}] \quad (2)$$

where f_{out} is the output frequency, W is a binary value for the FTW, f_{clk} is the operation clock frequency, N is the number of input bits of the phase accumulator, and INT[] denotes an integer part of the bracketed expression.

18. (New) The method of claim 15, wherein the binary value for the FTW comprises 010011001100110011001100110011001100110011001100110011001101, the number of input bits of the phase accumulator comprises 48, and the output frequency comprises 58.9824 MHz.

19. (New) The method of claim 15, wherein the square wave signal has a low jitter.

20. (New) The method of claim 15, wherein the system reference clock frequency is 19.6608 MHz and the operation clock frequency is 196.608 MHz.